

1. A memory array with byte-alterable capability comprising:

a select gate metal oxide semiconductor field effect transistor,

5 MOSFET device, and

102 a split-gate memory cell device whose source is connected to the  
drain of said select gate MOSFET device.

2. The memory array with byte-alterable capability of claim 1 further comprising:

10

102 bit lines which are tied to the drains of said split-gate memory  
cell.

3. The memory array with byte-alterable capability of claim 1 further comprising:

15

102 source lines which are tied to the sources of said select gate  
MOSFET devices.

4. The memory array with byte-alterable capability of claim 1 further comprising:

20

102 word lines which are tied to control gates of said split-gate memory  
cell.

5. The memory array with byte-alterable capability of claim 1 further comprising:

25

102 select lines which are tied to select gates of said select  
gate MOSFET devices.

102 6. The memory array with byte-alterable capability of claim 1 wherein said control gate MOSFET contains a floating gate which is insulated from said control gate by a dielectric insulating material such as silicon dioxide.

5

FIG 4

102

7. The memory array with byte-alterable capability of claim 6 wherein said split-gate memory cell contains a source region which is also the drain for said select gate MOSFET device.

102 8. The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a drain region.

102 9. The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a control gate which is insulated from said floating gate by a dielectric insulating material such as silicon dioxide.

102 10. The memory array with byte-alterable capability of claim 6 wherein said control gate contained in the control gate MOSFET device is insulated from said drain of said control gate MOSFET device by a dielectric insulating material.

20

102 11. The memory array with byte-alterable capability of claim 1 wherein said select gate MOSFET contains a select gate which is insulated from said select gate drain region and said select gate source region by a dielectric insulating material.

102 12. The memory array with byte-alterable capability of claim 1 wherein said bits of said bytes have a common source line.

col. 5, l. 42 5 13. The memory array with byte-alterable capability of claim 1 wherein said source lines common to said bytes have a high voltage applied to inhibit erase of said cells of said unselected bytes.

col. 5, l. 30 10 14. The memory array with byte-alterable capability of claim 1 wherein said source lines common to said bytes have a low voltage applied to enable an erase of said cells of said unselected bytes.

15 15. The memory array with byte-alterable capability of claim 1 wherein the erasure of selected bytes requires a high voltage on said select gates.

16. The memory array with byte-alterable capability of claim 1 wherein the erasure of selected bytes requires a high voltage on said control gates.

20 17. The memory array with byte-alterable capability of claim 1 wherein the programming of selected cells of said selected bytes require high voltage on said select gate, a lower voltage on said control gate and a high voltage on said source line.

18. The memory array with byte-alterable capability of claim 1 wherein said word lines common to said bytes have a zero voltage applied to inhibit programming of unselected cells.

5

19. A method of producing a memory array with byte-alterable capability comprising the steps of:

10                   including a select gate metal oxide semiconductor field effect transistor, MOSFET device, and.

                    including a split-gate memory cell whose source is connected to the drain of said select gate MOSFET device.

15   20. The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

                    including bit lines which are tied to the drains of said control gate  
20   MOSFET devices.

21. The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

25                   including source lines which are tied to the sources of said select gate MOSFET devices.

22. The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

5 including word lines which are tied to control gates of said control gate MOSFET devices.

23. The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

10 select lines which are tied to select gates of said select gate MOSFET devices.

15 24. The method of producing a memory array with byte-alterable capability of claim 19 wherein said control gate MOSFET contains a floating gate which is insulated from said control gate by a dielectric insulating material such as silicon dioxide.

20

25. The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a source region which is also the drain for said select gate MOSFET device.

25 26. The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a drain region.

27. The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a control gate which is insulated from said floating gate by a dielectric insulating material such as silicon dioxide.

5

28. The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate contained in the control gate MOSFET device is insulated from said drain of said control gate MOSFET device by a dielectric insulating material.

10

29. The method of producing a memory array with byte-alterable capability of claim 19 wherein said select gate MOSFET contains a select gate which is insulated from said select gate drain region and said select gate source region by a dielectric insulating material.

15

30. The method of producing a memory array with byte-alterable capability of claim 19 wherein said bits of said bytes have a common source line.

20

31. The method of producing a memory array with byte-alterable capability of claim 19 wherein said source lines common to said bytes have a high voltage applied to inhibit erase of said cells of said unselected bytes.

32. The method of producing a memory array with byte-alterable capability of claim 19 wherein said source lines common to said bytes have a low voltage applied to enable an erase of said cells of said unselected bytes.

- 5 33. The method of producing a memory array with byte-alterable capability of claim 19 wherein the erasure of selected bytes requires a high voltage on said select gates.

34. The method of producing a memory array with byte-alterable capability of  
10 claim 19 wherein the erasure of selected bytes requires a high voltage on said control gates.

35. The method of producing a memory array with byte-alterable capability of claim 19 wherein the programming of selected cells of said selected bytes  
15 require high voltage on said select gate, a lower voltage on said control gate and a high voltage on said source line.

36. The method of producing a memory array with byte-alterable capability of claim 19 wherein said word lines common to said bytes have a zero voltage  
20 applied to inhibit programming of unselected cells.